Beamforming

wave front

ΔΤ

processing
Assignment introduction

• Montium Tile Processor
Requirements

Montium TP

- Clock frequency the same as Montium TP
- Compatible with MontiumLLL compiler
  - configuration
  - control
  - DMA

CCU

- Smaller than 5% of Montium TP
- Critical path not inside CCU
- No buffering inside CCU for streaming interface
- Able to transfer data every clock cycle

MicroBlaze
Designed architecture
Designed architecture
ASIC resource usage

- Streaming control (47.5%)
- Crossbar (27.0%)
- DTL adapter (9.1%)
- Address decoder (5.3%)
- DMA input data multiplexer (2.6%)
- DMA interface (6.1%)
- Sequencer (2.4%)
Application
Application(2)

Montium

CCU

Network-On-Chip

MicroBlaze

Montium

CCU

MicroBlaze

DTL

streaming

DTL

streaming

DTL

DTL
Performance

- DTL write 2.65 MB/s
  - From MicroBlaze to Montium
- DTL read 0.99 MB/s
  - From Montium to MicroBlaze
  - Slower, because
    - 2 times communication over NoC necessary
    - Read takes more time in DTL adapter, due to memory access
Performance(2)

• Streaming interface
  – Maximum datarate 23.6MB/s per lane
  – 1 clock cycle latency

• Datarate dependent on communication scheme switching
  – 2 cycles delay when switching between communication schemes occurs
  – Datarate decreases to 7.97MB/s when between every transfer is switched between communication schemes
Conclusions

<table>
<thead>
<tr>
<th>Nr.</th>
<th>Description</th>
<th>Result</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.</td>
<td>Able to transfer data via streaming interface NoC</td>
<td>✔️</td>
</tr>
<tr>
<td>2a.</td>
<td>DTL interface for sequencer</td>
<td>✔️</td>
</tr>
<tr>
<td>2b.</td>
<td>DTL interface for config data</td>
<td>✔️</td>
</tr>
<tr>
<td>2c.</td>
<td>DTL interface for DMA transfer</td>
<td>✗️</td>
</tr>
<tr>
<td>3.</td>
<td>No buffering on streaming interface inside CCU</td>
<td>✔️</td>
</tr>
<tr>
<td>4.</td>
<td>Capable of transferring data every clock cycle on streaming interface</td>
<td>✔️</td>
</tr>
<tr>
<td>5.</td>
<td>CCU area smaller than 5% of Montium TP</td>
<td>✔️</td>
</tr>
<tr>
<td>6.</td>
<td>Clock frequency CCU same as Montium TP</td>
<td>✔️</td>
</tr>
<tr>
<td>7.</td>
<td>Critical path not inside the CCU</td>
<td>✔️</td>
</tr>
<tr>
<td>8.</td>
<td>Compatible with MontiumLLL</td>
<td>✔️</td>
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</tbody>
</table>
Recommendations

• More IP’s with streaming interface
  – ADC
  – DAC
  – Streaming memory

• DTL adapter improvement
  – Inside the CCU for higher datarates
  – Support for single Byte transfers
Questions?
Actual DMA write transfer, with value to be written at Montium input bus 1, dma_addr selecting the address to write to, bus_en selecting the local memory, and dma_rw is high to indicate a write.

Actual DMA read transfer, with value to be read at Montium output bus 1, dma_rw is low to indicate a read.
# FPGA resource usage

<table>
<thead>
<tr>
<th>Cell</th>
<th>Montium usage</th>
<th>CCU usage</th>
<th>DTL adapter usage</th>
</tr>
</thead>
<tbody>
<tr>
<td>Slice registers</td>
<td>3066</td>
<td>449</td>
<td>35</td>
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<tr>
<td>LUTs</td>
<td>15986</td>
<td>468</td>
<td>112</td>
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<tr>
<td>BRAMs</td>
<td>13</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>DSP48E1</td>
<td>5</td>
<td>0</td>
<td>0</td>
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